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RESEARCH ARTICLE

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A 1GS/s, 9-bits DAC Interleaved (2+1)-bit Then 2-bit per Cycle SAR ADC

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ABSTRACT

This study presents a high-speed successive-approximation-register analog-to-digital converter (SAR ADC) for low-noise low-power satellite transceiver applications. The proposed system is a (2+1)-bit then 2-bit per cycle SAR ADC with a sampling rate of 1 GS/s, 9-bits resolution designed in a 65-nm standard CMOS process. This system resolves nine bits using a special switching scheme in a total of four cycles per sample. This is achieved by interleaving four capacitive digital to analog converter (C-DACs) with 1-fF unit capacitance. As the interleaving is limited only to the DACs that match well, the design is not affected by the drawbacks of full interleaving. Hence, better power efficiency and performance metrics were obtained in comparison to regular interleaved ADCs. A special timing with an additional first bit comparator is optimized to have appropriate timing margins for every step from a single 4-GHz low-noise clock source that is readily available in the 8-GHz direct conversion frontend. This comparator is reused as the active comparator in both the interleaving phases. The proposed design achieved an effective number of bits value of 8.2 bits at Nyquist rate with a power consumption of 12 mW, resulting in a figure of merit of 38.37 fJ/conversion-step.

Keywords: ADC, high-speed, SAR

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Introduction

Successive-approximation-register analog-to-digital converters (SAR ADCs) were previously confined to medium-speed, medium-resolution applications as iterative sequential schemes required at least *n* number of cycles to resolve *n* number of bits. However, advances in technology and the various innovative architectures in the field made it possible to push the speed limits of the SAR ADC from hundreds of MS/s to few GS/s. Several approaches have been introduced to enhance the capabilities of SAR ADCs used for higher frequency applications. Moreover, SAR ADCs are considered as more power efficient than FLASH and pipeline as SAR ADCs depend primarily on digital logic and a single comparator that is considered to be the only active analog block in the circuit. Some systems incorporate asynchronous systems to eliminate any idle conversion time [1-4]. Differential SAR ADCs [1-3] are preferred over single-ended topologies [4] to enhance the linearity and to balance any possible mismatch. Differential SAR ADCs are achieved by doubling the capacitive DAC and increasing the switching power. The disadvantage associated with differential SAR ADCs in terms of power consumption was addressed by designing a monotonic switching scheme that resolves the same number of bits with less number of switching steps [1, 2]. Hence, this switching scheme has decreased the power consumption and reduced the area by half by excluding the MSB binary capacitor and resolving the first bit while sampling. However, it may severely suffer from the dynamic changes in the input common mode seen by the comparators. A trilevel monotonic switching SAR ADC [5] addressed the disadvantage of variations due to dynamic input common mode and suggested a switching scheme that keeps the input common mode voltage of the comparator constant.

Researchers have shown keen interest in interleaving SAR ADCs to resolve the speed constraint of single-stage ADCs; they increased the sampling speed by *n* number of interleaved stages. This was achieved by doubling the area and the power [6-9]. Although time interleav-

ing is widely used to enhance the speed, the linear relation between the sampling speed and the number of stages can result in lower performance due to channel-to-channel mismatches, thus limiting the number of stages that can be used. Some researchers have proposed the use of an extra channel for calibration [7], which is a less-preferred solution for low-power applications.

Another approach was introduced to increase the sampling rate using single-stage ADCs; multiple bits were resolved per cycle rather than 1 bit at a time. In the meantime, multi-bits-per-cycle SAR ADCs have been an area of interest to researchers [6], [10-13]. Multi-bit-per-cycle SAR ADCs can achieve higher

frequencies with less power, area, and circuit complexity compared with interleaving SAR ADCs with the only disadvantage of high power consumption due to the additional comparators. Reference [3] introduced a system that resolves 1-bit then 2-bit per cycle via top plate sampling method. The first bit can be identified immediately after sampling without waiting for any pre-charge operation.

The present study introduces an unconventional design technique based on (2+1)-bit then 2-bit per cycle SAR ADC with interleaving capacitive DACs, avoiding the complexity, high power consumption, and channel mismatches of conventional, fully interleaved SAR ADCs. The proposed method shown in Figure 1 significantly enhances the speed–resolution tradeoffs via multi-bit cycling with special timing and an additional comparator. The rest of the paper is organized as follows. Section II provides a detailed explanation of the system architecture and switching scheme. Section III describes circuit implementation for various sub-blocks. Simulation results and performance metrics of the proposed system are presented in Section IV, and Section V concludes the study.

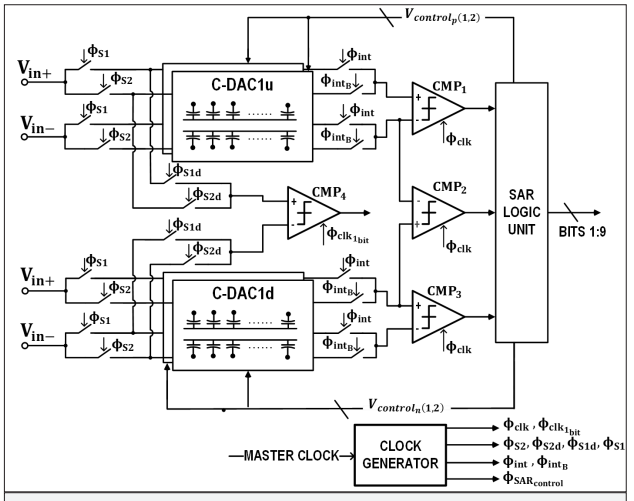

Figure 1. Block diagram of the proposed system

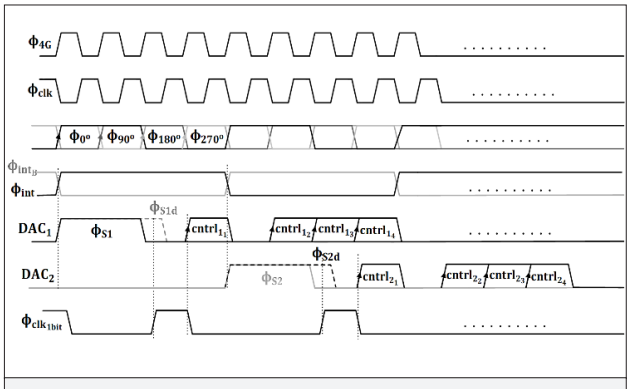

Figure 2. Detailed system-timing diagram

Proposed SAR ADC Architecture and Switching Scheme

Timing of the proposed (2+1)-bit then 2-bit per cycle SAR ADC with interleaving DAC is shown in Figure 2. The system block diagram is illustrated in Figure 1. It primarily comprises four differential binary weighted DACs for bit cycling operation, three comparators for defining the four regions of comparison needed to resolve two bits at a time, and an additional comparator that operates at one fourth of the master-clock frequency to identify the first bit. Moreover, sampling switches, DAC interleaving switches, a synchronization block, and a SAR control unit are required to control the capacitive DAC operation to dump the equivalent charge based on the decision at the previous step.

System Architecture

The main advantage of this work is that interleaving the DACs reduces the number of comparators and sampling duration without any significant change in performance and power consumption. This approach has additional advantages: it increases the sampling period and addresses the settling-time constraint for the most significant first conversion step. The two DACs; DAC_1, DAC_2, are interleaved with the clocks ϕ_{int} and ϕ_{int_S}. Taking DAC_1 as an example, when clock ϕ_{ints} is low, it is disconnected from the backend cycling comparator system. Simultaneously, clock ϕ_{s1} turns on for the sampling phase to take place, where the input is differentially sampled on the top plates of DAC_1 array while all their bottom plates are recharged to common mode voltage (V_{cmi}). Meanwhile, DAC_1 is connected to the first bit comparator *(CMP$_4$)* when ϕ_{s1d} clock is high. The signal ϕ_{s1} goes low slightly earlier, allowing the sampling node to settle and hold. Then, $\phi_{clk\text{-}1bit}$ is fired to take the first bit decision; this switch should be disconnected from the sampling node before dumping any charge to avoid voltage degradation resulting from charge distribution. On the contrary, DAC_2 executes the 2-bit-at-a-time resolving scheme through the backend cycling comparators. When clock ϕ_{int_S} goes high, the DAC_1 array is connected to this backend comparator array to start resolving two bits at a time with $cntrl1_{2,3,4}$ rising edges, as shown in Figure 2. DAC_2 repeats the same operation with ϕ_{int} clock in control of sampling; then, 1-bit resolution when ϕ_{int} goes low, followed by 2-bit cycling until a total of nine bits are resolved.

Timing and Switching Scheme

The timing diagram illustrated in Figure 2 shows the control signals of every block in the system. A 4-GHz master clock is available in the system. A timing block is implemented to generate a 1-GHz clock in its four phases used to sample the output bits at the speed of two bits per rising edge of each of the four phases of the clock. Moreover, a 500-MHz clock is needed to control the interleaving switch and generation of the control signals for each SAR control unit controlling the interleaving DACs. The conversion sequence of this SAR logic is summarized in Figure 3.

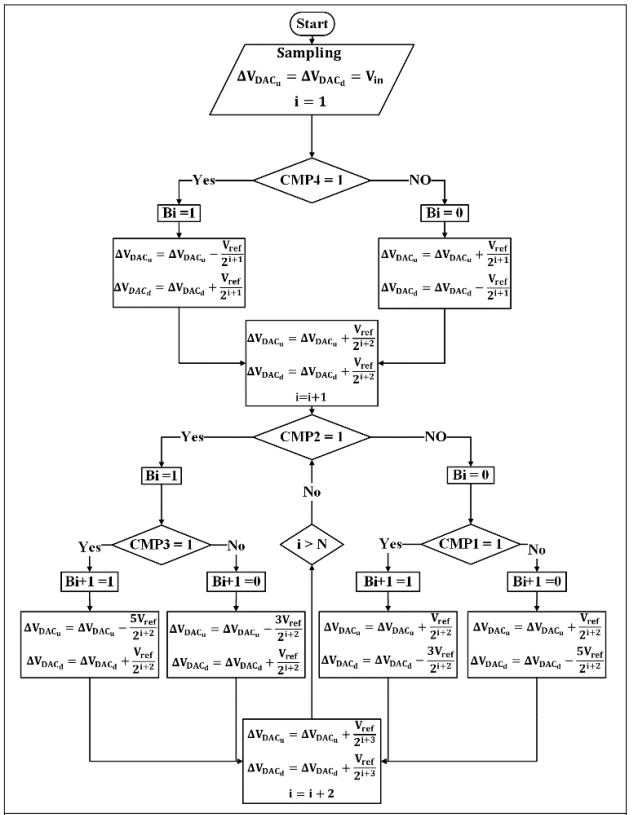

Figure 3. Flowchart for the switching scheme of a single DAC

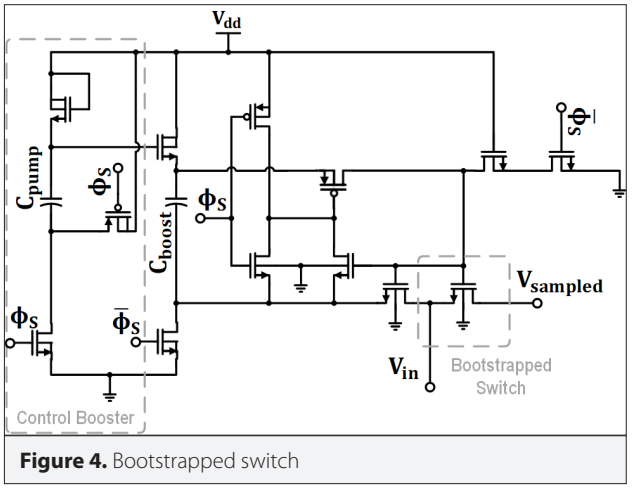

Figure 4. Bootstrapped switch

Circuit Implementations

This section discusses the details of the circuit blocks.

Sampling and Interleaving Switches

Sampling switches are considered as one of the most critical blocks for high-speed ADC applications. The sampling switch

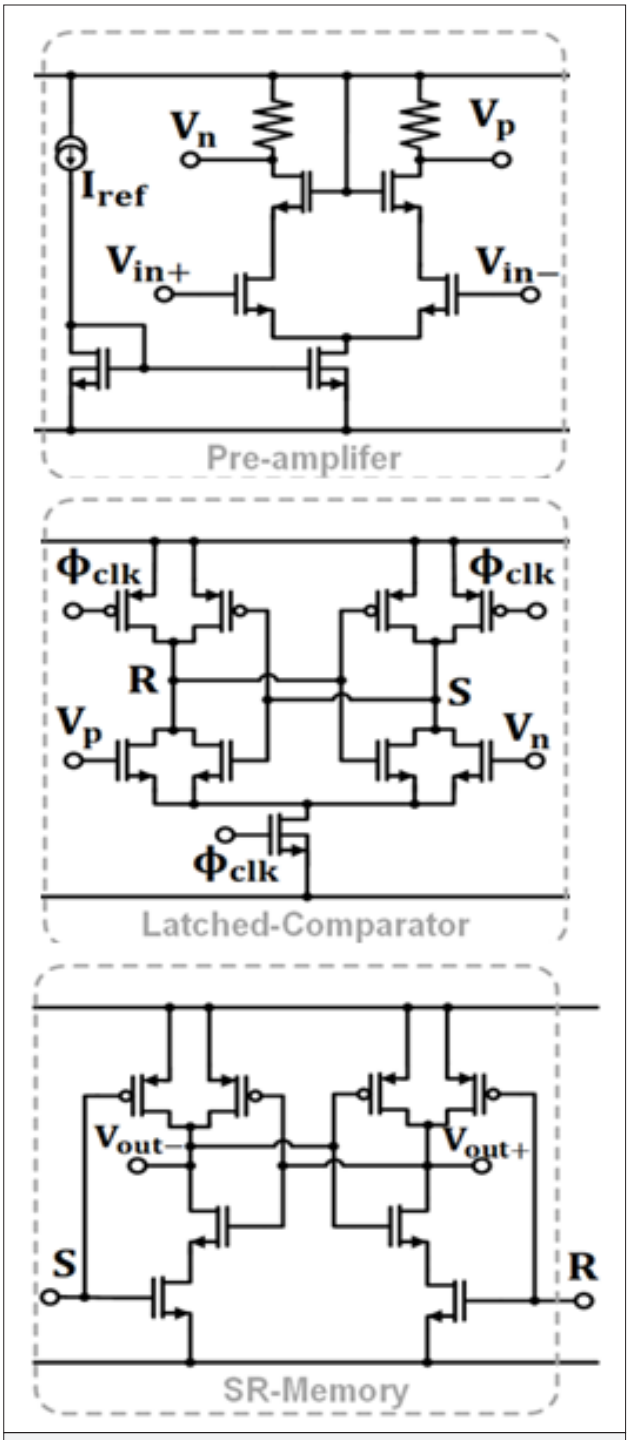

Figure 5. Comparator Circuit Design

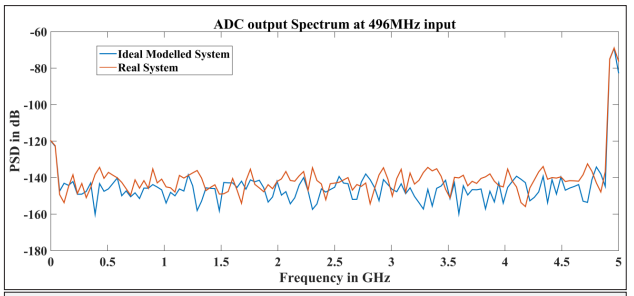

Figure 6. Frequency response at Nyquist rate

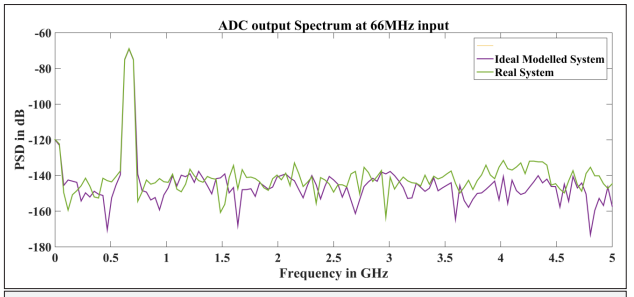

Figure 7. Frequency response at 66.4 MHz

Table 1. Font sizes and styles

Publication	[6] IJSSC'18	[10] ISCAS'14	[11] CICC'17	This Work
Architecture	2XTI -2b SAR	SAR	SAR	(2+1) then 2b SAR –DAC TI
Technology	28 nm	65 nm	40 nm	65 nm
Supply(V)	0.9	1.2	1.2	1.25
Resolution	7 bits	8 bits	10 bits	9 bits
f_s (GS/s)	2.4	0.4	0.3	1
Unit Cap. (F)	-	2.5f	0.5f	1f
Total Cap. (F)	64f	4*640f	935*0.5f	4*256f
Power (mW)	5	5.6	2.1	12
Figure of merit (fJ/conv.-step)	25.3	67f	19	38.374

linearity plays a crucial role in defining the overall linearity of the system. Thus, it should be carefully designed for good overall linearity. The ON resistance of NMOS switches is dependent on the source gate voltage (V_{GS}); this makes this resistance dependent on the input signal. This dependency can be expressed using Equation (1). Moreover, the threshold voltage V_{th} of the sampling device also depends heavily on the input voltage.

$$R_{nmos_{on}} = \frac{1}{\mu_n C_{ox} \frac{W}{L}(V_G(t) - V_{in}(t) - V_{th}(t))} \quad (1)$$

Bootstrapped switch scheme was implemented to provide a constant V_{GS} (across the bootstrapped switch) as high as Vdd, keeping the value of "ON" resistance constant [14] and ensuring linear performance for the switch design shown in Figure 4. The proposed system comprises three clocked switches: sampling switches, 1st bit sampling switches, and interleaving switches. All the three are bootstrapped switches with sizes proportional to their sampling capacitance.

Comparator

A schematic of the comparator is shown in Figure 5. It is a latched comparator with a high-speed pre-amplifier with low-offset diff-pair cascode gain. This stage is designed for a fixed current of 800 uA per comparator. The 1K ohm load resistors belonging to the four comparator preamplifiers are used as a trim point during power-up single-time DC offset calibration.

Simulation Results

The entire system is simulated using Cadence CAD tool along with the extracted capacitive DAC array to include the parasitic effects. Figure 6 shows the output spectrum of the ADC at full Nyquist rate; Figure 7 shows the response to a 66.4-MHz input.

Conclusion

The performance summary of the proposed design are summarized in Table 1; the results of previous experiments are included in the table for reference. An untraditional SAR approach proposed in this study provided a unique opportunity for a low-power, robust ADC design in a 65-nm CMOS circuit with simple quadrature clock phases. Utilizing only one additional comparator and by doubling up the passive C-DACs with corresponding interleaved timing, an effective number of bits value of 8.2 bits was achieved with total current consumption of <10mA from a single power supply of 1.25 V.

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Conflict of Interest: The authors has no conflicts of interest to declare.

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